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DATA ACQUISITION FOR THE CDF SVX II UPGRADE

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ABSTRACT

CDF is developing a second generation silicon vertex detector for the Fermilab Tevatron Run II. In order to exploit the high luminosity of the Fermilab Main Injector, the data acquisition system is being designed to accept high trigger rates and accommodate a secondary vertex trigger.

1. Introduction

The Collider Detector at Fermilab (CDF) has successfully operated the first silicon vertex detector (SVX) at a $p\bar{p}$ collider. The SVX has been a critical component for the study of top and bottom physics, primarily by allowing the detection and measurement of secondary vertices. The Fermilab Collider Run II will follow the Main Injector upgrade which will increase the luminosity to about $10^{32}/\text{cm}^2/\text{s}$. In order to reduce the number of collisions per crossing, the number of bunches in the machine will be increased and the time between interactions reduced from 3500 ns to 396 ns, and ultimately to 132 ns. This shortening of the interaction time necessitates the redesign of the vertex detector data acquisition system (DAQ) and a rebuild of the detector.

In addition to accommodating the accelerator upgrade, this new detector, SVX II, is being redesigned to accomplish a number of physics goals. SVX II will significantly improve the vertexing, resolution, and acceptance of the vertex detector. This is done primarily by increasing the over-all length of the detector by nearly a factor of two and by employing double-sided sensors.¹ In addition, a very important goal of SVX II is to provide data to a secondary vertex trigger (SVT) being developed for CDF.² This could have a great impact on the B physics capability of CDF by, for example, allowing the triggering of $B \rightarrow \pi\pi$.

The front end integrated circuit chip (SVX II chip) is being designed for both the CDF and D0 experiments to handle 396 ns and 132 ns beam crossings.³ In order to accommodate the shortened interaction time, the front end electronics must store the data during the initial (level 1) trigger decision time. The latency time of the level one trigger is a fixed 4.2 μsec requiring a pipeline 32 cells deep for 132 ns operation. The control of this chip and the data handling is the primary task of the rest of the

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system. To limit electromagnetic interference (EMI) to other CDF sub-detectors, the data read-out is accomplished by fiber optics. Furthermore, the components of the system inside the detector must be radiation hardened and low mass.

2. SVX II Chip

The SVX II chip is designed to read-out both polarities of AC-coupled, double-sided detectors. The chip consists of four main sections. For each of 128 channels there is a charge integrating preamplifier, switched-capacitor pipeline, and ADC. This is followed by a digital section with sparse read-out. The front end integrator requires several (132 ns) beam crossings to reset. Consequently, the preamplifier has a large dynamic range ($350 \text{ fC} \approx 87 \text{ mip}$) allowing the integrator to be reset during the abort gaps in the accelerator cycle. The integrator rise time can be adjusted to optimize signal-to-noise for 396 ns and 132 ns operation. The chip is designed to achieve an rms equivalent noise of 1700 e for 132 ns operation with 20 pF source capacitance. The signal-to-noise of the detector is expected to be in the range of 10~15:1. The switched capacitor pipeline has a programable depth up to 32 cells. The pipeline layout uses a mirrored design that eliminates channel cross-talk and maximizes available area for the capacitors. Digitization is performed at 106 MHz by means of an on-chip ramp generator and external 53 MHz clock. Digitization time for 7 bits is thus $1.2 \mu\text{sec}$. A ramp pedestal allows the adjustment of the threshold to 400 e resolution. The read-out proceeds over an 8 bit data bus.

3. Distributed Control

The SVX II chip has four modes of operation: initialization, acquisition, digitization, and read-out. These modes are set by mode lines and driven by an external, differential clock (SVX II clock). The SVX II clock has a variable frequency and duty cycle depending on the chip mode. The chip is initialized by 182 bits of configuration data. During acquisition, digitization and read-out, real time control of internal reset switches is performed over the 8 bit data bus.

The control of the SVX II chip is distributed between three pieces of hardware: read-out controller (SRC), fiber interface (FIB), and port card PC (see figure 1). The port card is located just outside the SVX II space frame, buried deep inside the CDF detector. The distributed design features minimal control lines and PC logic that is simple enough to be implemented in a radiation hard FPGA. The firmware of this FPGA stores the sequences for real time control of the SVX II chip, but the timing is driven by an external, serial clock (SR-CLK in figure 1). Most of the complex logic for driving the chip is in the FIB which produces the SVX II clock and the serial clock. The FIB resides in a VME crate allowing many diagnostics to be performed. High level commands to the SVX II chip originate in the SRC as a parallel command sent to a fan-out in the FIB crate. The SRC interfaces to the CDF trigger and synchronizes the SVX II DAQ to the accelerator beam crossings.

4. Data Read-out

Upon receipt of a (level 1) trigger, the data is digitized from the corresponding pipeline cell and read out into buffer cards (SAR in figure 1) in the SRC VME crate.

The data is read out in parallel, segmented along the beam direction and in 30° degree azimuthal sections called wedges. The 28 chips of each wedge are daisy-chained into 3 buses. The data is stored in the SAR buffers until the next-level trigger decision (level 2), and can be simultaneously input into the SVT. It is important to minimize the time it takes to get the data into the SVT, as this adds to the trigger decision time. Since the SVT will use only the $r-\phi$ data, the chips connected to $r-\phi$ strips must be read out first. This is handled by appropriately routing the chip daisy-chain. The time to read-out the data depends on the number of chips in a bus and the worst wedge channel occupancy, and is expected to be about $3\ \mu\text{sec}$. During digitization and read-out, the chip is not acquiring data. In addition, there is a dead-time due to the pipeline buffer equal to the pipeline depth times the interaction time ($4.2\ \mu\text{sec}$ @ 132 ns). The total dead time is expected to be about $8\ \mu\text{sec}$ at the 132 ns interaction time.

Optical fibers are preferred for the data read out because they do not produce EMI and they have minimal mass. However, an electrical-optical interface using LED lasers cannot be put directly on the detector because of heat and space considerations. Rather, this interface is made on the PC which also serves to regulate chip power. Thus, the data path, from chip to SAR buffer, goes over three distinct links. A microstrip cable with a high line density (high density interconnect, HDI) carries the data from the chips to the PC at 53 Mbytes/s over 8 parallel lines. The short ($\sim 10\ \text{cm}$) length of the HDI allows the data to be driven directly off of the SVX II chip to the PC, and limits EMI and cable mass. On the PC the data is converted to 8 parallel optical fibers in a dense electrical-optical connection (dense optical interface module, DOIM). Industry is just beginning to produce these devices and they are still very expensive. The industry module that comes closest to meeting our needs is made by Hitachi.⁵ We are developing a custom version that is pin compatible with the Hitachi model and that is potentially lower power and lower mass. The DOIM transfers the data at 53 Mbytes/s over 10 meter, multimode fibers to the FIB. From the FIB, the data must be transferred to SAR buffer cards located some 70 meters away in the counting room. In order to reduce the number of long fibers, the data is serialized (16:1) at the FIB. This is done using the Hewlett Packard G-LinkTM chipset.⁴ The G-Link chip set is a highly integrated, compact, bipolar silicon device that functions as a transparent "virtual" 16 bit ribbon cable with a band-width of up to 1.5 Gbits/s. The serialized data will be transmitted optically using optical driver and receiver modules from Finisar which can reliably transmit data over large distances.

5. Status and Prospect

Work is proceeding to build test components for all the read-out hardware. These components will be integrated into a test stand. The test stand development will aid in component integration issues, software development, as well as providing a means to read-out SVX II chips for chip studies, detector studies, laser testing of detectors, a test beam, and production testing of sub-assemblies. The test stand software is being written for a front-end, VME-embedded CPU card running real-time UNIX and connected via ethernet to a host computer.

In order to fully exploit the high B cross section at the tevatron and make use of the triggering capabilities of the SVT trigger, it is necessary to sustain high level 1 trigger rates— as high as 50 kHz. At high trigger rates, the dead time associated with the

SVX II chip becomes large (40% @ 50KHz). For this reason, work is proceeding towards the development of a deadtimeless chip (SVX III). The pipeline for the SVX III will be dual ported, allowing simultaneous reading and writing. A skip logic architecture is being developed to prevent over-writing of cells that have been triggered. In order to reduce noise coupling from the digital operations into the active analog front end, the data lines will be differentially driven and the chip will be split into separate analog and digital chips. The HDI will need to be redesigned to accomodate SVX III. However, the changes to the rest of the system should be minimal, due to the high degree of flexibility built into the system by the distributed control architecture and the use of programable logic.

References

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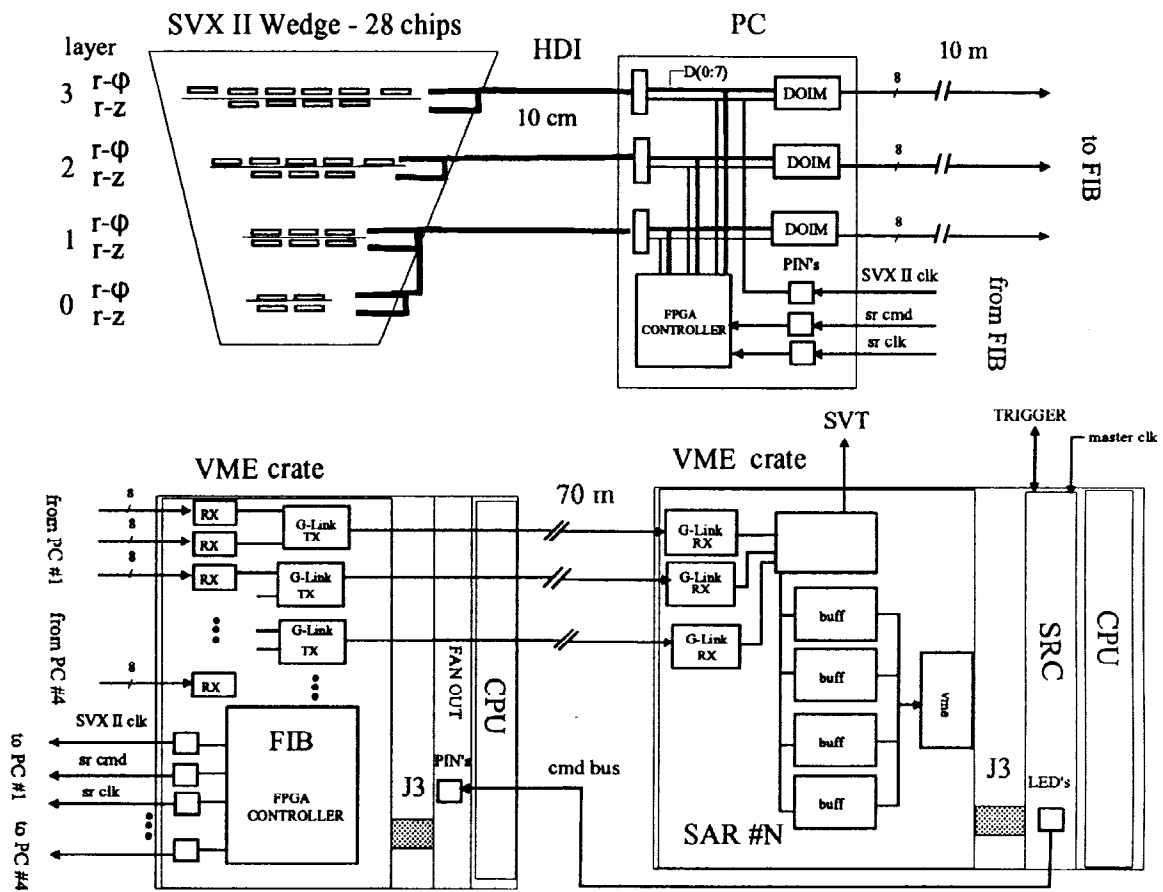


Fig. 1. Overview schematic of the SVX II data acquisition system.